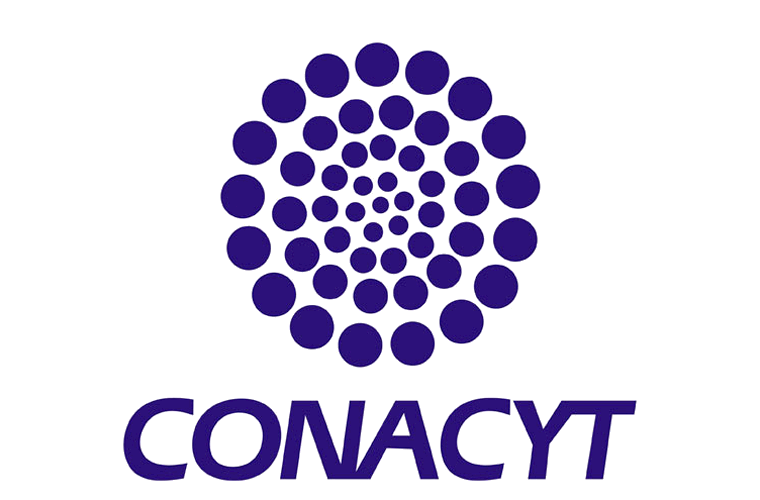
** **

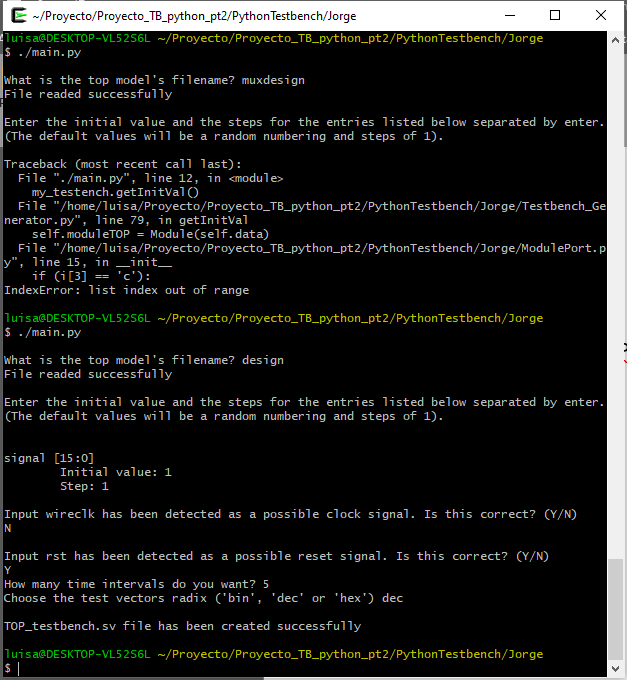
**Testbench Generator for Verilog code, implemented in Python.**

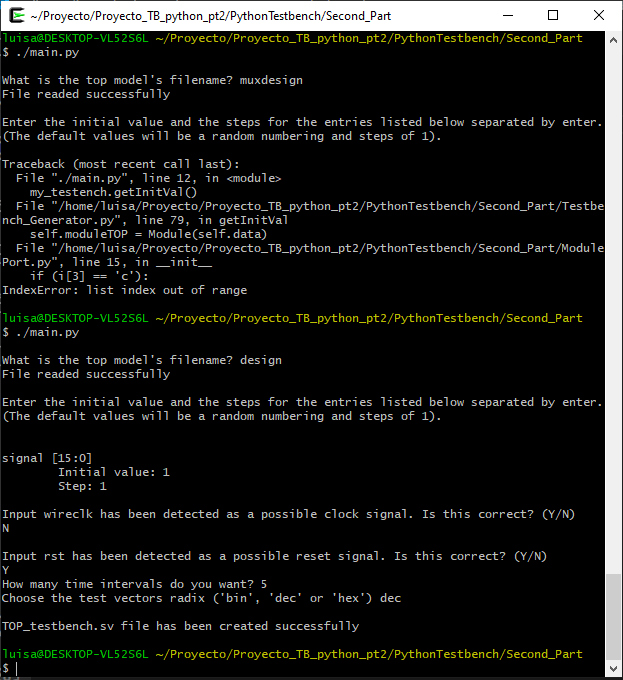
**Part 2**

**Professor: Carolina Rosas Huerta**

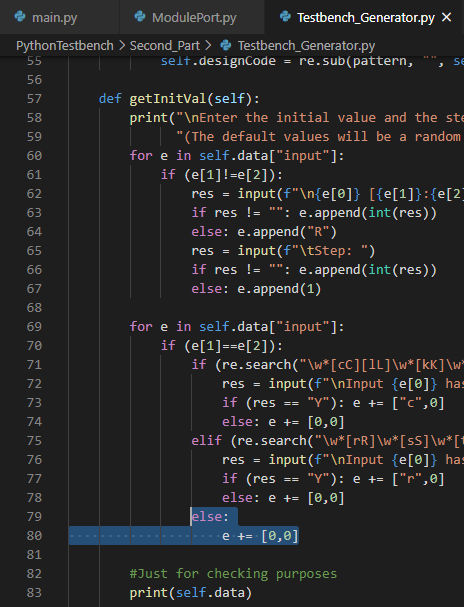
# **Notes (11 nov).**

* The “Second\_Part” folder was created in order to host the files corresponding to the Second Part of this project. This folder initially has the same files as the ones in Jorge’s folder (his code is the base for the Second Part).
* Jorge’s code already has a loop that enables the user to type the correct Verilog design’s name in multiple tries.
* The Python interpreter was set to Python version 3.6 in order to run inside Fernando’s machine.
* Error detected. When the Verilog design “design.sv” is fed to the program, it runs correctly, but when the Verilog design “muxdesign.sv” is fed, the program does not work (see next page). SOLUTION AFTER THE IMAGES





* Solution: in method “getInitVal(self)”, add an ‘else’ after the clock and reset search to append [0,0]



self.data of muxdesign (before solution):

{'module': [['Logic\_mux2', 0, 0]], 'input': [['a', 0, 0], ['b', 0, 0], ['c', 0, 0]], 'output': [['y', 0, 0]]}

self.data of design:

{'module': [['TOP', 0, 0]], 'input': [['wireclk', 0, 0, 0, 0], ['rst', 0, 0, 'r', 0], ['signal', 15, 0, 1, 1]], 'output': [['PC\_Out', 0, 31], ['Imemo\_Inst', 0, 31], ['RAM\_Rw', 0, 31], ['RAM\_R1', 0, 31], ['RAM\_R2', 0, 31], ['ALU\_Flag', 0, 0]]}

self.data of muxdesign (after solution):

{'module': [['Logic\_mux2', 0, 0]], 'input': [['a', 0, 0, 0, 0], ['b', 0, 0, 0, 0], ['c', 0, 0, 0, 0]], 'output': [['y', 0, 0]]}

* Error detected. The Test vectors do not change value when the Verilog design “muxdesign” is used.

